An Improved Power Quality SMPS using Power Factor Corrected Zeta Converter

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***Abstract*—Normally, multiple-output Switched Mode Power Supplies (SMPSs) for Personal computers (PCs) depict extremely bad power quality indices at the utility interface such as total harmonic distortion (THD) of the input current being more than 80%, power factor being lower than 0.5 and output voltage regulation being very poor. The limits of harmonic emissions set by international power quality standards are being violated in such cases. A non isolated power factor corrected (PFC) Zeta converter is being used here at the front end to improve the power quality of an SMPS for a PC. The front-end converter is able to reduce the ripple in its output that is being fed to the second stage isolated converter. The performance of the front-end Zeta converter is evaluated in three different operating conditions. The performance of this SMPS has been simulated here.**

Keywords—Multiple outputs, power factor corrected Zeta converter, power quality, switched mode power supply (SMPS), unity power factor.

I. INTRODUCTION

Personal computers (PCs) have become an inevitable part of our day- to-day activities. Switched Mode Power Supply (SMPS) is an integral part of the personal computers that converts ac to multiple numbers of suitable dc voltages to impart power to different parts of the PC. It consists of a diode bridge rectifier (DBR) with capacitor filter, whose charging and discharging causes high distortions in input currents, followed by an isolated dc-dc converter. This also increases neutral current in distribution systems if large number of PCs are used that causes noise, derating of transformer, voltage distortion and results in disruption in the computer system performance[2]-[5].

Single stage power factor corrected (PFC) converter can achieve high power factor and voltage regulation at the same time and has good reliability, but limited rating about 200W. For medium rating, two stage SMPS is used, first to improve power quality and second for regulated dc output voltage. For high quality power supply, both power factor (PF) and total harmonic distortion (THD) are important. Discontinuous conduction mode (DCM) offers lower THD for input current than continuous conduction mode (CCM) and also offers low cost, reduction in number of sensors and component size. Basic converters include buck, boost, buck-boost, Cuk , Sepic and Zeta[6]-[7]. Boost operates only as step up voltage and is not capable of protecting itself against load over current or short circuit. Cuk and Sepic which can be operated as step down and step up voltage do not protect themselves against overload and have design issues .All the above converters require an additional circuit to limit the inrush current. Buck has the capability of naturally limiting inrush current and protecting against overload but difficult to operate at high PF and high rms current stress and has limited output voltage range. Buck-boost operates as step down or step up converter and is capable of limiting both load and inrush current, but have pulsating output current. Zeta converter, when operating in DCM, draws a line current proportional to input voltage with no harmonic contents and it provides high PF, overload and short circuit protection. It has limited inrush current and output voltage is regulated using only one active switch.

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II. PFC ZETA CONVERTER BASED SMPS CONFIGURATION

Fig.1 shows the system configuration of a PFC Zeta converter based multi-output SMPS topology. At the input, a DBR with filter is connected to a non-isolated Zeta converter. It consists of two inductors L_{z1} and L_{z2}, one intermediate capacitor C_1, one high frequency switch S and one diode D. This PFC converter regulates the output dc voltage and draws a sinusoidal current from the ac mains at unity PF. Three different DCM conditions (i.e., input inductor (L_{z1}) in DCM, intermediate capacitor in DCM and output inductor (L_{z2}) in DCM) are considered here. In the DCM operation, the current becomes zero either in the input inductor or output inductor, or the voltage across the intermediate capacitor becomes zero for some duration in one switching cycle. The output dc voltage is regulated using a Proportional-Integral (PI) voltage controller. The regulated output dc voltage is connected to an isolated converter for achieving multiple dc voltages at the output. The isolated converter consists of two equal valued input capacitors, two switches, one high frequency transformer (HFT) and filters. The filters are used in each output winding to reduce the output voltage and current ripples. Only one of the output voltages is directly sensed and the other output voltages are controlled by the duty cycle of the isolated converter. The winding that is selected for control action is of

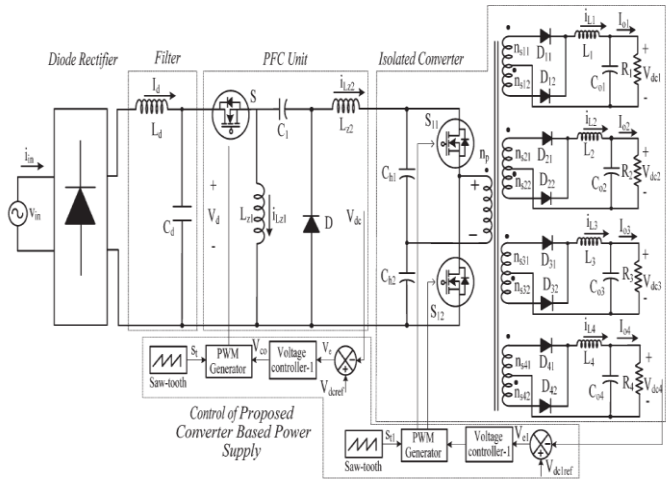

Fig. 1. PFC Zeta converter based SMPS for PCs

the largest power rating among all the outputs. Further, to reduce the component stresses, the isolated converter is designed in CCM. Another voltage PI controller is used here to regulate the output voltage.

III. OPERATING PRINCIPLE

The operation of the proposed SMPS is studied to analyze its behaviour in one switching cycle. Three different conditions have been considered for the PFC Zeta converter.

A. PFC Converter when input inductor is in DCM

When switch S turns on, inductors, L_{z1} and L_{z2} charges and capacitor C_1 discharges. When S is turned off, diode D conducts, stored energy in L_{z1} starts decreasing and continues until current i_{Lz2} equals the negative of current i_{Lz1} and C_1 charges. When both S and D are off, the state lasts until the start of next PWM cycle and i_{Lz1} remains zero ensuring DCM condition.

B. PFC Converter when intermediate capacitor is in DCM

When switch S is on, inductors, L_{z1} and L_{z2} charges with intermediate capacitor C_1 discharging through L_{z2}. When S is in conduction state, C_1 is completely discharged and voltage across C_1 becomes zero ensuring DCM. L_{z2} continues to supply energy to the output capacitor. When S is off, L_{z1} discharges through C_1 and L_{z2} discharges through isolated converter.

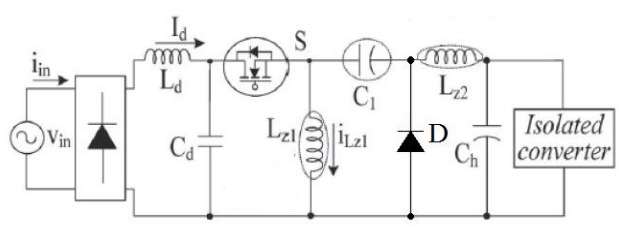

Fig 2.Magnified Zeta converter

C. PFC Converter when output inductor is in DCM

When S turns on, L_{z1} and L_{z2} charges and C_1 discharges. When S is turned off, energy in L_{z1} is transferred to C_1, L_{z2} feeds isolated converter. This stage continues until i_{Lz1} equals negative of i_{Lz2}.When switch S and diode D are off, the state lasts until the start of next PWM cycle. The output inductor current remains zero ensuring DCM.

Isolated converter used here is a half bridge converter working in CCM and is described in two states during one half of the switching cycle where upper switch is involved and in second half lower switch is involved.

IV. CONTROL OF CONVERTERS

The front end converter is controlled using voltage follower approach while isolated converter uses average current control. The control of the front end PFC converter generates pulses according to the output voltage error (V_e) which is the difference between desired voltage and reference voltage. V_e is fed to PI controller to generate controlled output voltage (V_{co}).

$$V_{co}(n)=V_{co}(n-1)+k_pV_e(n)-V_e(n-1)+k_iV_e(n) \quad (1)$$

where k_p and k_i are proportional and integral gains.

The output of PI controller is compared with a high frequency saw-tooth signal to generate PWM pulses. If the output voltage varies, the control output voltage, V_{co} changes to vary the duty cycle. Hence the width of PWM pulses changes accordingly to maintain the dc output voltage. To control the multiple dc output voltages of isolated converter, average current control scheme is used. Output voltage error is given as input to PI controller and its output is compared with saw-tooth wave to generate switching pulses.

V. DESIGN

The design is based on the change in the inductor current during the switch on and off period. The relation between output voltage V_{dc} and input voltage, V_{in} of zeta buck-boost converter is expressed as

$$\frac{V_{dc}}{V_{in}(t)} = \frac{D}{1-D} \quad (2)$$

A. Input inductor selection

The critical inductance value of input inductor is

$$L_{z1min} = \frac{D(t)TV_{in}(t)}{2I_{in}} \quad (3)$$

To design L_{z1} in CCM

$$L_{z1min} = \frac{D(t)TV_{in}(t)}{\Delta i_{in}(t)} \quad (4)$$

B. Output inductor selection

The critical value of output inductor is

$$L_{z2min} = \frac{\big(1-D(t)\big)TV_{dc}}{2I_{dc}} \quad (5)$$

To design L_{z2} in CCM

$$L_{z2min} = \frac{(1 - D(t))TV_{dc}}{\Delta I_o} \quad (6)$$

C. Intermediate capacitor selection

Value of intermediate capacitor is calculated as

$$C_1 = \frac{D(t)TV_{dc}}{2V_{C1}R_{dc}} \quad (7)$$

To design C1 for CCM is given by

$$C_1 = \frac{D(t)TV_{dc}}{2\Delta V_{C1}R_{dc}} \quad (8)$$

VI. SIMULATION RESULTS

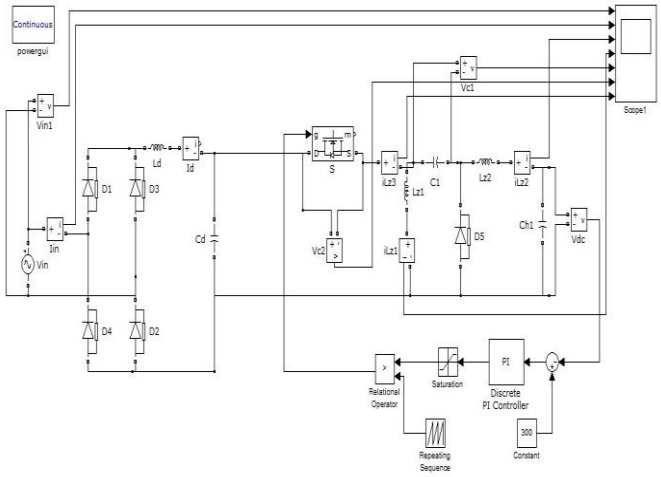

Fig 3. Simulink model of power factor corrected zeta converter

The performance of the proposed Zeta converter based SMPS is studied through simulation results and is modelled in MATLAB/Simulink. The performance is analyzed in three operating conditions.

Fig. 4, Fig. 5 and Fig. 6 show the waveforms of input voltage(v_{in}), input current (i_{in}), current through input inductor(i_{Lz1}), current through output inductor (i_{Lz2}), voltage across intermediate capacitor (v_{C1}), voltage stress across switch S(V_S) and current stress across switch S(I_S) during different operating conditions in DCM. In Fig.3 the current through the output inductor i_{Lz2} and voltage of the intermediate capacitor V_{C1} remain in continuous conduction while the current in input inductor is in DCM. In Fig 4, it is clearly seen that V_{C1} remains discontinuous for some time in one switching cycle while the currents in input and output inductors (i_{Lz1} and i_{Lz2}) remain continuous. When L_{z2} is operating in DCM corresponding current touches zero in each PWM cycle as in Fig. 5.

From the simulated results it is clear that all the three operating conditions is well within the international power quality limits. The voltage stresses for L_{z1} and L_{z2} in DCM are quite acceptable than C_1 in DCM. Peak current is slightly lower when L_{z2} is operating in DCM which makes it more suitable for PC application. Moreover the current in input

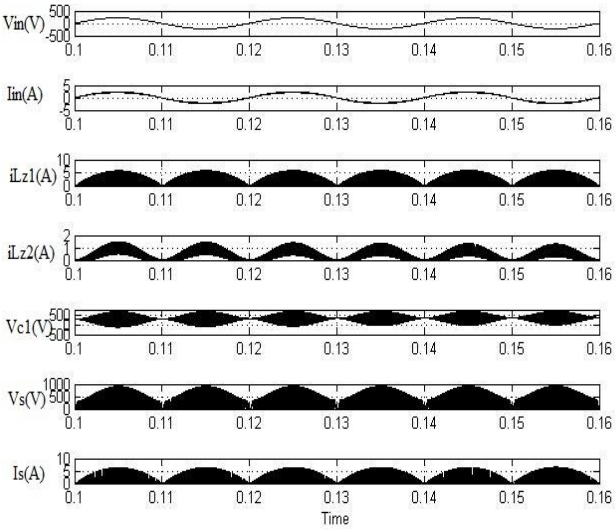

Fig 4. Waveform of PFC converter when L_{z1} is operating in DCM

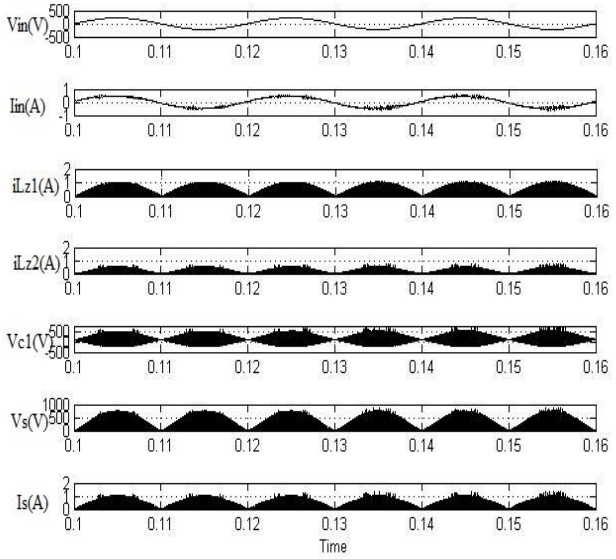

Fig 5.Waveform of PFC converter when C_1 is operating in DCM

inductor L_{z1} and voltage across intermediate capacitor V_{C1} are maintained in CCM .Power factor when L_{z1} in DCM is 0.9982,when C_1 in DCM is 0.9557 and when L_{z2} in DCM is 0.9995 .

Total harmonic distortion in all the three cases are less than 10% and are well within the international power quality limit.

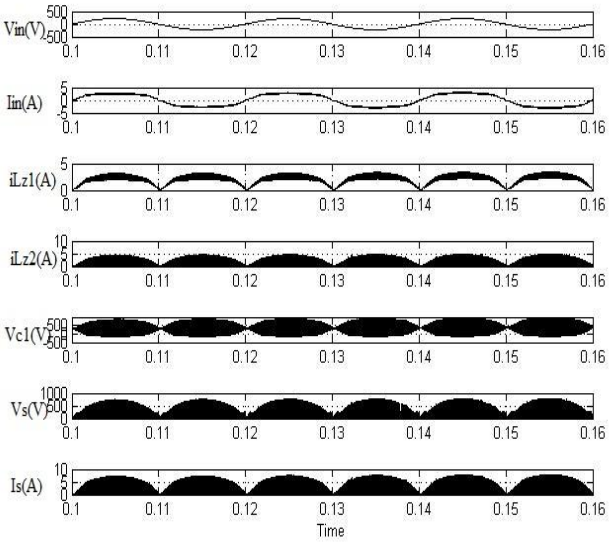

Fig 6. Waveform of PFC converter when L_{z2} is operating in DCM

VII. CONCLUSION

DCM operated front-end PFC converter cascaded with a multiple output isolated converter has been used for the design of an SMPS for PCs. It has been modelled and simulated for input power quality improvement and output voltage regulation. The simulation in three different modes of operation of the front-end converter have been carried out to analyse the performance of SMPS based on device stresses and are within the international power quality limit.

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